Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1. (previously presented) A receiver comprising:

analog-to-digital circuitry for generating a digital representation of an amplified analog signal at an input;

adjustable gain control circuitry for receiving a radio signal and outputting the amplified analog signal using a gain determined directly by a bit signal at an output of the analog-to-digital circuitry; and

digital channel filtering circuitry for filtering said digital representation; and digital processing circuitry for processing the output of said digital channel filtering circuitry.

Claim 2. (cancel)

Claim 3. (previously presented) The receiver of claim 1 wherein said gain is reduced by a first amount responsive to a most significant of said bit signal indicating that the analog-to-digital converter has exceeded a first saturation threshold.

4. (previously presented) The receiver of claim 3 wherein said adjustable gain control circuitry reduces said gain independent of said digital processing circuitry.

5. (previously presented) The receiver of claim 3 wherein said gain is reduced by a second amount responsive to a set of most significant bits of said bit signal indicating that the analog-to-digital converter has exceeded a second

saturation threshold.

6. (previously presented) The receiver of claim 1 wherein said gain is increased responsive to a set of most significant bits of said bit signal indicating that the analog-to-digital converter is below a threshold.

7. (currently amended) A method of receiving a radio signal in a receiver, comprising the steps of:

generating a digital representation of a signal at an output of a analog-to-digital converter after applying a gain to the radio signal;

adjusting the gain by a control directly connected and responsive to bit values of the digital representation of said output of said analog-to-digital converter;

generating a filtered digital representation for a desired channel; and

processing the filtered digital representation.

8. (cancelled)

9. (previously presented) The method of claim 7 wherein said adjusting step includes adjusting the gain by a first predetermined amount responsive to the value of a most significant bit of said bits values.

10. (original) The method of claim 9 wherein said adjusting step includes the step of adjusting the gain by a second predetermined amount responsive to a set of most significant bits of said bit values.

11 – 12 . (cancelled)

13. (previously presented) A receiver comprising:

adjustable gain control circuitry for receiving a radio signal and outputting an amplified analog signal using a gain determined directly by a single sample of

digital representation at an output of an analog-to-digital (ADC) circuitry;

digital channel filtering circuitry for filtering said digital representation; and digital processing circuitry for processing the output of said digital channel filtering circuitry.

14. (previously presented) The receiver of claim 13 wherein said adjustable gain control circuitry is coupled to receive an output signal from at least one low pass filter.

15. (previously presented) The receiver of claim 14 wherein at least one input of said at least one low pass filter is coupled to an output of at least one mixer.

16. (previously presented) The receiver of claim 15 wherein at least one input of said at least one mixer is coupled to an output of an amplifier.

17. (previously presented) The receiver of claim 16 wherein an input of said amplifier is coupled to an output of a bandpass filter.

18. (previously presented) The receiver of claim 14 wherein said at least one low pass filter comprises two low pass filters.

19. (previously presented) The receiver of claim 13 wherein said adjustable gain control circuitry comprises two gain control circuits, whereby both sensitivity and interference tests may be conducted.

20. (previously presented) The receiver of claim 13 wherein at least an MSB bit of said digital representation at said output of the analog-to-digital circuitry is directly connected to an input of said adjustable gain control circuitry.

21. (previously presented) The receiver of claim 13 wherein said analog-

to-digital circuitry comprises two analog-to-digital circuits, one of said analog-to-digital circuits having an output directly connected to an input of said adjustable gain control circuitry, whereby both sensitivity and interference tests may be conducted.

22. (previously presented) The receiver of claim 1 wherein said gain is operable to be reduced and increased by different thresholds, respectively, whereby hysteresis is prevented.

23. (previously presented) The method of claim 7 comprising a further step of reducing and increasing said gain by different thresholds, respectively, whereby hysteresis is prevented.

24. (previously presented) The receiver of claim 13 wherein said gain is operable to be reduced and increased by different thresholds, respectively, whereby hysteresis is prevented.

25. (new) The receiver of claim 1 wherein said gain is reduced by a first amount responsive to a most significant of said bit signal, free of counting a number of the most significant of said bit, indicating that the analog-to-digital converter has exceeded a first saturation threshold.